

Introduction to Digital Annealer

Fujitsu Quantum-Inspired Computing

Digital Annealer

[Technical Edition]

Fujitsu Limited

Patented including related technologies

Fujitsu Quantum Inspired Technology: Digital Annealer





Classification of Quantum/Quantum-Inspired Computers FUjiTSU

Based on the difference in operating principles, it is classified into an Ising Machine method and a Quantum Gate method.

Digital Annealer solves combinatorial optimization problems using Ising Machine Method.
 Extremely low temperatures or high vacuum are not required.



Solving Combinatorial Optimization Problems with Ising Model

- Find the state of X (ground state) that minimizes the energy of the system, converting the spin state of the Ising model into binary variables

 D(U)
 DU
 DU
 - $E(X) = -\sum_{i,j} W_{ij} x_i x_j \sum_i b_i x_i$ State X= (x₁, x₂, ..., x_i, ..., x_N) State variable of bit i x_i \in {0,1}
- Three elements for handling combinatorial optimization problems with Ising Model
 - ✓ Number of bits
 - Degree of coupling between bits
 - Coupling strength gradation between bits

for optimization





What is Annealing Method?



• An algorithm based on the annealing metal processing phenomenon

Annealing Phenomenon

A phenomenon in which a metal is heated to a high temperature and then cooled slowly to a stable structure (low energy)



Check all the combination by moving up in order to go back if a combination does not work



Annealing Method

Find a way to quickly fit all the pieces by shaking the whole system significantly, then gradually decreasing the degree of shaking



The search for the optimal solution begins with solutions that are far from the optimal, then progress to a solutions that are closer to the optimal solution.



A quantum inspired computing technology that enables fast solution of combinatorial optimization problems which are difficult to solve with current general-purpose computers.

Features

1. Large-scale

Addresses the 100,000-bit problems (1M-bit at research level)

2. Faster

Annealing core^{*1} incorporates search technology that utilizes constraint conditions to speed up the solution of many complex actual problems

3. High convenience

•Separate input of cost terms and constraint terms allows automatic adjustment of constraints coefficient during the search

•Linear inequality constraint terms can be entered directly without QUBO*2

^{*1:}A search engine that repeatedly performs bit inversion based on an annealing method *2:QUBO (Quadratic Unconstrained Binary Optimization)

Reason of High Speed of 4th Gen



*Digital Annealing Unit

Basic Principle of Annealing Core



Probabilistic search performed in parallel

3rd Gen

- Constraint exploitation Search (Software) starts DAU by dividing the problem considering the constraints
- Medium size (~8,192 bit) problem is solved by dedicated chip

4th Gen

- Can perform bit processing without dividing the problem by large-scaled annealing core
- Utilizing constraint conditions at the selection of inverted bit, flip 2/4bits simultaneously on 1/2way1hot constraints.





What is Digital Annealer 4th Gen?

A large-scale annealing core solves optimal solutions at high speed while keeping the convenience of the 3rd Gen.

• Faster solving of large-scale problems

Max 10 times faster than 3rd Gen with large-scale annealing cores (multi-GPU)

Convenience

- A new API which reduces QUBO formulation of 1-hot constraint^{*1}. It reduces input data and complexity.
- The use of Azure BLOB Storage^{*2} supports handover of large sized problem.
 Max Problem size: 3rd Gen 2GB, 4th Gen 20GB

*1: A common constraint in real problems such as scheduling problems

*2: Separate contract by customer required

*3: Binary Quadratic Programming (BQP)



Convenience: Digital Annealer API



Automatic adjustment of constraints term coefficient

Separate input of complex constraints and simplifies tuning



Automatic adjustment of coefficient *a* reduces tuning

Inequality Constraints Support

Reducing the number of auxiliary bits by providing inequality constraints separately from the cost term



Supports multiple inequality constraints without the auxiliary bit y_n

1hot Constraints Support

Quick processing of typical constraints for 1 hot constraints that are frequently used in real world problems 1 way-1 hot Constraints





Select only one bit which becomes "1" in the target group

The 4th generation does not need Binary Quadratic Constraint term (1hot group must be specified as in the 3rd generation)



Supplement (Roadmap)

Technology Roadmap

* The contents of the roadmap are subject to change without prior notice







Thank you

Digital Annealer Public Site

https://www.fujitsu.com/global/services/business-services/digital-annealer/